

Notice of References Cited	Application/Control No. 10/735,123	Applicant(s)/Patent Under Reexamination KELLER ET AL.	
	Examiner Russell Frejd	Art Unit 2128	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,253,361	06-2001	Buch, Premal	716/6
*	B	US-6,587,815	07-2003	Aingaran et al.	703/13
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	BLAAUW et al., D. Driver Modeling and Alingment for Worst-Case Delay Noise, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 11, No. 2, April 2003, pp. 157-66.
	V	CHEN et al., W-C. Analytical Models for Crosstalk Excitation and Propagation in VLSI Circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 21, No. 10, October 2002, pp. 1117-31.
	W	SASAKI et al., Y. Crosstalk Delay Analysis of a 0.13- μ m Node test Chip and Precise Gate-Level Simulation Technology, IEEE Journal of Solid-State Circuits , Vol. 38, No. 5, May 2003, pp. 702-8.
	X	PHADOONGSIDHI et al., M. A Concurrent Fault Simulation for Crosstalk Faults in Sequential Circuits, Proceedings of the 11th Asian Test Symposium , November 2002, pp. 182-7.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.